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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	5

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,449	BAILIS ET AL.	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Claim Objections

2. Claim 9 objected to because of the following informalities: There are two colons ":" ending the preamble. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "at least one point of interest" is indefinite and does not clearly define "what" is the point of interest. More clarification is required.

4. Claims 6 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "signals of interest" is indefinite and does not clearly define "what" are the signals of interest. More clarification is required.

5. Claim 9 recites the limitation "the at least one bus" in the debug client function. There is insufficient antecedent basis for this limitation in the claim. The limitation should read "a at least one bus" or "at least one bus".

6. Claims 10-15 are rejected because they depend on claim 9 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (US-6260087), or Chang1, in view of Barnett (US-6173419) and further in view of Chang (US-5687325) or Chang2.

Claim 1:

Chang1 teaches in Fig. 1, a PCI Bus Controller ("PCIBC") ASIC 10 (ASIC). Chang1 also teaches included in the PCIBC 10 are conventional functional blocks (standard cell including a plurality of logic functions) include a SRAM block 12, an EEPROM or Flash Memory block 14, a FIFO block 16, a RISC processor or DSP block 18, and a PCI bus interface block 22 (internal bus with internal signals). In principle, the RISC processor or DSP block 18 can be any type of central processing unit ("CPU") including a DSP, a micro-controller, RISC or a complex instruction set computer

("CISC"). (Col. 5, lines 33-43). Chang1 also teaches the PCIBC 10 includes a programmable logic block (PLB) 26 (a FPGA function). (Col. 5, lines 56-58). Chang1 does not explicitly teach that the PLB 26 has a debug function, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10. (Col. 5, lines 65-67; col. 6, lines 1-5). As previously mentioned, Chang1 also discloses a RISC processor or DSP block 18 which can be any type of central processing unit ("CPU") including a, a micro-controller. Chang1 further teaches a Smart Card Controller ("SCC") ASIC in Fig. 2. Barnett teaches an emulator that may be used to emulate a micro-controller in a smart card. FPGA 100 is programmed with a model of a micro-controller 102 and a model of monitoring or debug logic 104 (debug client function). (Col. 5, lines 37-43). Barnett further teaches monitoring or debug logic 104 provides the logic surrounding micro-controller 102 that allows a fully transparent window into the internal functioning of micro-controller 102 and observe the signals and timing at any point in the micro-controller (observe signals). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang1's PLB 26 program with Barnett's debug function in FPGA 100 to observe signals. The artisan would be motivated to do so because it would enable Chang1 to have more control of the micro-controller in observing the signals and timing at any point. Chang2 teaches of a FPGA included within an ASIC that is configurable to effect a specific digital logic circuit interconnection between fixed functional units (manipulates bus signals). (Col. 3, 32-37; col. 5, lines 66, 67; col. 6, lines 1-19). It would have been obvious to one of ordinary skill in the art at the

time the invention was made to also configure Chang1's PLB 26 as Chang2's FPGA to manipulate the signals of the Chang1's conventional functional blocks. The artisan would be motivated to do so because it would enable Chang1 to have more control of the micro-controller in manipulating the data presented on Chang2's bus interface 26.

Claim 9:

The debug client function with an ASIC and a FPGA is rejected as per claim 1. The modification of Chang1's PLB 26 with Barnett's FPGA to include the debug function is presented in the rejection of claim 1. Also, The limitation of "selector logic coupled to the at least one bus and the plurality of internal signals" is rejected per claim 1.

Chang1 does not explicitly teach PLB 26 includes an external communication logic function for receiving and transmitting information to a server, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10, one being a PCI bus interface block 22. (Col. 5, lines 65-67; col. 6, lines 1-5). Chang1 also teaches a CPU (not illustrated in any of the FIGS.), that is included in the computer system (server), communicates with the RISC processor or DSP block 18 (also a micro-controller, programmed into the PLB 26 per Barnett, claim 1) through the PCI bus interface block 22 (Also programmed into the PCB 26). An in-system programming ("ISP") interface 28, included in the PLB 26, provides a port through which the PLB 26 may be programmed or configured (debug client function programmed by a server). (Col. 6, lines 35-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Chang1's PLB 26 could be programmed to implement the function of the PCI bus

interface block 22 (external communication logic function). The artisan would be motivated to do so because this would enable the debug client function programmed in the PCB 26 (per Barnett) to communicate with the server.

Chang1 does not explicitly teach PLB 26 includes an interface logic, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10. (Col. 5, lines 65-67; col. 6, lines 1-5). Chang2 teaches that the FPGA 48 may also be configured to perform additional logic functions (interface logic). (Col. 6, lines 19-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Chang1's PLB 26 could be programmed to implement Chang2's additional logic functions (interface logic). The artisan would be motivated to do so because this would enable Chang1 to create additional logic to interface between Chang2's bus selector circuit and Chang1's PCI bus interface block 22 (external communication logic function).

Claim 2, 10:

The limitation of "the at least one bus comprises an internal bus" is rejected per claim 1.

Claim 3, 11:

The limitation of "the debug client function observes and manipulates at least one point of interest on the standard cell" is rejected per claim 1.

Claim 4, 12:

The modification of Chang1's PLB 26 with Barnett's FPGA to include the debug function is presented in the rejection of claim 1. Chang1 teaches a CPU (not illustrated

in any of the FIGS.), that is included in the computer system (server), communicates with the RISC processor or DSP block 18 (also a micro-controller) through the PCI bus interface block 22. An in-system programming ("ISP") interface 28, included in the PLB 26, provides a port through which the PLB 26 may be programmed or configured (debug client function programmed by a server). (Col. 6, lines 35-45). Barnett also teaches the host computer (server) compiles the source level logic descriptions of the microprocessor 102 and debug interface 104 (debug client function) and loads and configures them into the field programmable gate array (FPGA). (Col. 7, lines 30-35).

Claim 5:

The modification of Chang1's PLB 26 with Barnett's FPGA to include the debug function is presented in the rejection of claim 1. Also, The limitation of "selector logic coupled to the at least one bus and the plurality of internal signals" is rejected per claim 1.

Chang1 does not explicitly teach PLB 26 includes an external communication logic function for receiving and transmitting information to a server, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10, one being a PCI bus interface block 22. (Col. 5, lines 65-67; col. 6, lines 1-5). Chang1 also teaches a CPU (not illustrated in any of the FIGS.), that is included in the computer system (server), communicates with the RISC processor or DSP block 18 (also a micro-controller, programmed into the PLB 26 per Barnett, claim 1) through the PCI bus interface block 22 (Also programmed into the PCB 26). An in-system programming ("ISP") interface 28, included in the PLB 26,

provides a port through which the PLB 26 may be programmed or configured (debug client function programmed by a server). (Col. 6, lines 35-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Chang1's PLB 26 could be programmed to implement the function of the PCI bus interface block 22 (external communication logic function). The artisan would be motivated to do so because this would enable the debug client function programmed in the PCB 26 (per Barnett) to communicate with the server.

Chang1 does not explicitly teach PLB 26 includes an interface logic, however, Chang1 does suggest that the PLB 26 can implement one or more functions that is performed by the functional blocks included in the PCIBC 10. (Col. 5, lines 65-67; col. 6, lines 1-5). Chang2 teaches that the FPGA 48 may also be configured to perform additional logic functions (interface logic). (Col. 6, lines 19-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made that Chang1's PLB 26 could be programmed to implement Chang2's additional logic functions (interface logic). The artisan would be motivated to do so because this would enable Chang1 to create additional logic to interface between Chang2's bus selector circuit and Chang1's PCI bus interface block 22 (external communication logic function).

Claim 6, 13:

The modification of Chang1's PLB 26 with Barnett's FPGA to include the debug function is presented in the rejection of claim 1. The limitation "and output logic function..." is rejected per claim 5 above (external communication logic function). Barnett teaches in FIG. 8 that shows an example of the logic found in the debug

interface 104. Barnett suggests that emulators (see claim 1 for combination) have trace memory that stores the addresses and data values (storage logic function) that the micro-controller has used while running. The host software can then examine this (provided to the server). Barnett teaches a comparator 142 (comparator logic function) which compares the break address from the break register 140 with the address stored in the code ROM (signals of interest).

Claim 7, 14:

Barnett teaches host computer 136 contains a source level debugging software program that cooperates with the logic (hardware) in debug interface 104 to allow the software engineer to execute software code instructions in the target environment and observe the signals and timing at any point in the micro-controller. (Col. 6, lines 19-24).

Claim 8, 15:

Barnett teaches Ram 106 holds the code store that provides a program for operating the modeled micro-controller 102. A host computer 108 holds a debug program for debugging the code store software (debug software) provided to micro-controller 102.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gupta (US-6577158)

Gupta teaches input/output blocks (external communication logic) and programmable interconnects (select logic) embedded in a FPGA 115. (Claim 5).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

Albert DeCady
Primary Exami[illegible]